Heavy Ion Testing of the Motorola Nano-crystal Nonvolatile Memory

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I. Introduction

The purpose of the test was to determine the SEE sensitivity of the Motorola nano-crystal nonvolatile memory. The test was performed at the Texas A&M University cyclotron.

II. Devices Tested

The test chips were engineering samples of 4M (512K x 8) nonvolatile memories fabricated using Motorola technology targeted on the 90 nm node. These were based on Si nano-crystals, or floating gate technology. The floating gate samples represent the next generation of today's mainstream commercial flash technology, while the nano-crystal technology is a new approach that may eventually replace floating gate. The nano-crystal technology has been described in more detail, elsewhere [1]. There were five samples, each, of these types.

III. Test Facility

Facility: Texas A&M University Cyclotron Single Event Effects Test Facility, with 15 MeV/nucleon tune.
Fluence: 10^7 particles/cm^2
Flux: Average flux varied from 8.94×10^4 to 2.95×10^5 particles/cm^2-s.

Ion	E(MeV)	LET (MeV/mg/cm^2)	Range (?m)
Ar	497	8.7	175
Kr	916	29.3	117
Xe	1299	53.8	102

IV. Test Methods

The NASA test system was built to exercise the chips, according to documentation provided by Motorola. Hak Kim and Mohammed Suhail and other Motorola employees consulted regularly during the development of this test system. The chips were all packaged in a standard test package, and had common pin assignments, as described in documentation supplied by Motorola. The intention was to test in the static mode, as well as dynamic read, program and erase modes. That is, a pattern was written with the

beam off; then the sample was exposed to the beam; and then read again to detect any changes. Dynamic read testing was similar except that the pattern was read continuously during the exposure, and the errors counted. The program and erase tests were not conducted because programming and erasing were difficult without the beam on, and usually took longer than the exposure. The original plan was to cycle continuously through program/read/erase/read, and count errors when the pattern read differed from the pattern expected. Patterns that could be written were all zeroes, all ones, checkerboard, and inverse checkerboard. Most of the testing was actually done with zeroes written, since that was the state sensitive to radiation. For the nano-crystal memories in the read mode, V_G was around 3.3-V, although the exact voltage varied slightly from sample to sample, and V_D was 2.2-V. The power supply for the program/erase operations was +/- 6-V. For the floating gate samples in read mode, V_G was 5.5-V, and V_D was 4-V. Program/erase voltages were +/- 9-V. Programming was accomplished by channel hot electron (CHE) injection, and erasing was by Fowler-Nordheim (FN) tunneling. The program and erase voltages were supplied from an external power supply.

V. Results

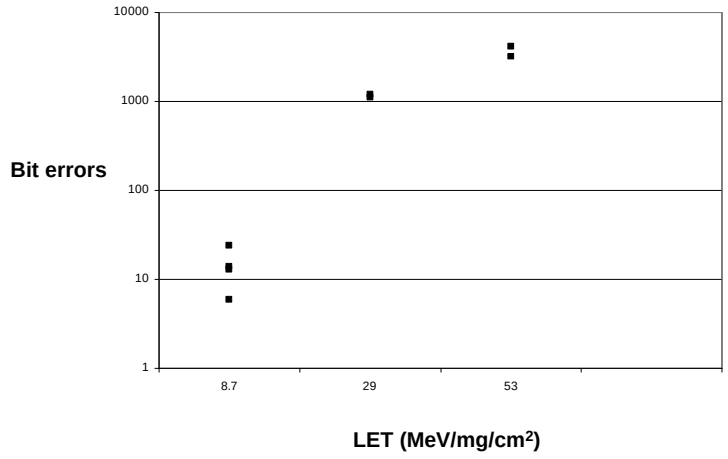
The results of the static tests and the dynamic read tests are very similar in the number of errors produced at a given LET, which suggests that the errors are all static bit flips. That is, there appear to be no errors due to transients in the peripheral circuits. All the testing was done at relatively low frequency, so the failure to capture any SETs is not surprising. All the static bit flips are zeroes turned into ones. When the cell is written into the zero state, electrons are injected into either the floating gate or the Si nano-crystal layer. The usual effect of ionizing radiation in a MOS structure is to introduce positive trapped charge in the oxide, which reduces the net effective negative stored charge, either by compensation or by recombination. For this reason, the threshold voltage (V_T) is reduced for transistors hit by an ion. If the threshold voltage is reduced below some critical value, the bit is read as a one (gate empty of electrons) rather than as a zero (gate full of electrons).

For the floating gate technology, only one part was tested, and no errors were observed, at LET = 29.3. The pattern was checkerboard, so only half the bits were in the zero state. Total particle count was $2x10^7$ ions/cm^2.

For the nano-crystal technology, the results for stored zeroes are summarized in Figure 1, and in Table I. The static and dynamic read tests produced similar results, leading to the conclusion that all the errors were really static, except that there was some double counting in the dynamic tests. That is, some errors were read more than once in the dynamic test. However, the double counting has been eliminated in Fig. 1, since it could be identified from the data log. The erase and write tests were not performed because the parts were difficult to write and erase, even with the beam off. Usually it took two or three successive write or erase operations to get all the bits written or erased, which took far longer than the exposure time. There would have been no way to tell if the errors observed after a short exposure were due to the effects of the ion beam, or because the

write/erase was incomplete. For the read tests illustrated in Fig. 1, the maximum bit error count was slightly more than 4000, for 10^7 particles/cm^2. However, the area of the memory array is much less than a square cm, perhaps 0.2 cm^2. Therefore, the number of ions hitting the array is on the order $2x10^6$ per exposure. Perhaps 27 or 28 percent of the array area is active gate area (estimated from a SEM picture), so the number of ions hitting active gate regions is about $5x10^5$ per exposure. In other words, less than one ion out of 100 that hits the active gate area changes the state of the cell, even at the highest LET tested so far. Therefore, the observed cross section is about 0.01 times the geometric gate cross-section, or $1.2x10^{-12}$ cm^2/bit. The results in Fig. 1 do not indicate saturation of the cross-section with LET yet. However, examination of the data log indicates about 7000 combined bit errors for all exposures at LET = 53, but only about 5000 word address errors. That is, about 40% of the words with one error also had a second error. Reasons for this result are unclear. If less than one ion in 100 that hits the active gate area causes an error, it seems unlikely that any ion would cause more than one error. Perhaps weak bits come in clusters. The underlying mechanism for the bit errors appears to be related to the micro-dose—an ion deposits a small, dense cluster of positive charge, which neutralizes enough of the stored electrons on the storage element to change the state of the cell. However, Cellere et al. [2] reported that the negative charge lost off floating gate devices irradiated with heavy ions was far greater than the amount of positive charge deposited by an ion. For this reason, the underlying mechanisms are not completely clear, and should be the subject of further study.

Fig. 1



No latchup (SEL) was observed at any point in the testing. The highest LET was 53, and the total number of ions incident at that LET was $5x10^7$/cm^2. Therefore, the maximum latchup cross-section is on the order of $2x10^{-8}$ cm^2.

VI. Recommendations

The basic nano-crystal technology looks promising for space applications, but it needs to be tested in the program and erase modes, which are expected to be more sensitive to radiation than the read mode tested here.

References:

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2. G. Cellere, A. Paccagnella, L. Larcher, A. Chimenton, J. Wyss, A. Candellori, and A Modelli, *Anomalous Charge Loss from Floating-Gate Memory Cells Due to Heavy Ion Irradiation*, IEEE Trans. Nucl. Sci., **NS-49**, 3051 (2002).